**CpE 2210 Homework Assignment #4**

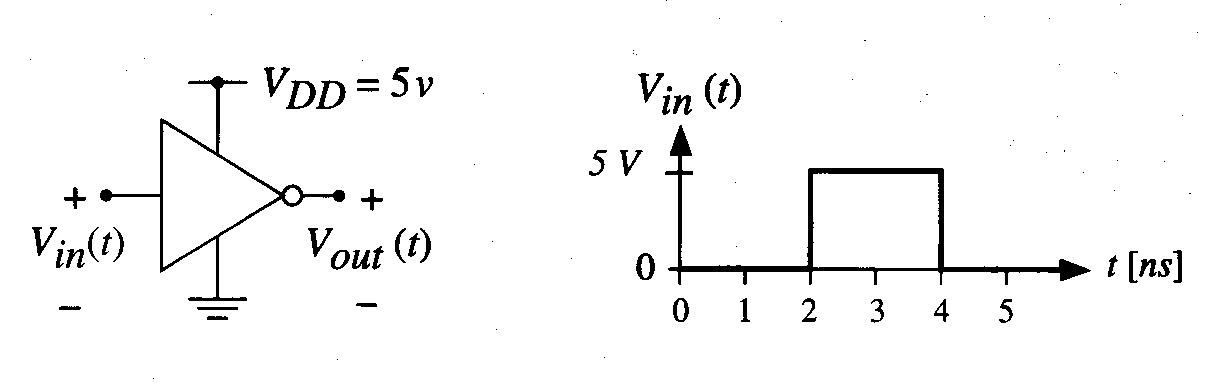
HW#4 is due at the beginning of class on Friday, March 22. You must always show or explain your work in a neat and orderly format. You are encouraged to discuss ideas with other students and consult references but your work must be your own.

1. An inverter (NOT) gate is designed with tHL=0.25ns and tLH=0.5ns. The input voltage Vin is shown in accompanying figure, and is known that the output voltage ranges from Vout=0v to Vout=5v. (15pts)

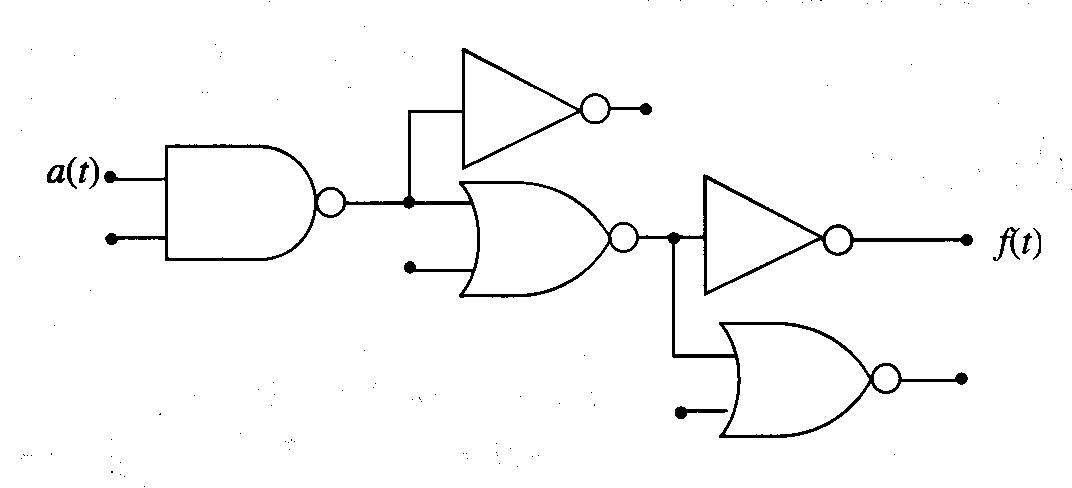
(a) Draw a waveform for Vout(t).

(b) What is the maximum switching frequency for this circuit, if 90% and 10% of VDD are used as threshold voltage levels for logic 1 and 0, respectively? Draw a waveform of the output voltage Vout at this frequency.

(c) Suppose that the input is driven at twice the maximum frequency. Draw a waveform of the output voltage in this case, and explain why the gate will not operate properly.



2. Calculate the delay between the input signal *a(t)* and the output *f(t)*, using the following parameters: tp0,NOT = 0.5ns, tpL,NOT = 0.4ns, tp0,NOR = 0.75ns, tpL,NOR = 0.9ns, tp0,NAND = 0.85ns, tpL,NAND = 0.95ns. Assume that the output drives the input to one inverter.



3. Construct 4:1 MUX using only 2:1 MUXs as the main building blocks.

4. Use an 8:1 MUX to implement the function

5. Perform the following binary additions without using decimal equivalents. (15pts)

(a) 1100 0110 + 0100 1100

(b) 1101 0000 + 1010 1010

6. Perform the following subtractions by translating into binary and applying the 2s

complement approach. Use word size of 9b (i.e., 9-bit signed binary integer). (15pts)

(a) 15 – 6

(b) 196 – 114

7. Perform the following binary multiplications. (15pts)

(a) 1011 x 1011

(b) 1110 x 0110

8. Design a transmission gate network that implements the function